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Thermodynamic stability of $Ga_2O_3(Gd_2O_3)$/GaAs interface

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$Ga_2O_3(Gd_2O_3)$/GaAs heterostructures have been annealed up to ~780 °C. Studies using x-ray reflectivity and high-resolution transmission electron microscopy have shown that the samples annealed under ultrahigh vacuum have maintained smooth and abrupt interfaces with the interfacial roughness being less than 0.2 nm. The oxide remains amorphous, an important parameter for device consideration. Current–voltage and capacitance–voltage measurements have shown low leakage currents (10^{-8}–10^{-9} A/cm^2), a high dielectric constant of 15, and a low interfacial density of states (D_{it}) between gate dielectrics and GaAs. The attainment of a smooth interface between the gate dielectric and GaAs, even after high temperature annealing for activating implanted dopant, is a must to ensure the low (D_{it}) and to maintain a high carrier mobility in the channel of the metal–oxide–semiconductor field-effect transistor. © *2005 American Institute of Physics*.
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Today's integrated circuits are based on Si metal–oxide–semiconductor field-effect transistor (MOSFET) technology. A GaAs MOSFET offers potential advantages over a Si-based MOSFET because of the high electron mobility, high breakdown field, and semi-insulating substrate of GaAs. Searching and identifying electrically and thermodynamically stable insulators on GaAs with a low interfacial density of states (D_{it}) has been one of the key challenges in the compound semiconductor devices over the past four decades.[1,2] *In situ* deposition of $Ga_2O_3(Gd_2O_3)$ dielectric film on GaAs surfaces produced MOS diode structures with a low D_{it}.[3,4] Subsequent employment of the $Ga_2O_3(Gd_2O_3)$ as a gate dielectric along with an ion implantation process led to the demonstration of the first enhancement mode GaAs MOSFETs with inversion on semi-insulating GaAs substrates in both *n*- and *p*-channel configurations.[5]

Previously, the oxide-GaAs interface was found to be roughened in a high temperature (>750 °C) annealing for fabricating the inversion-channel GaAs MOSFETs,[5,6] in which the annealing was inevitably needed to activate the ion implantation for ohmic contacts at source and drain regions. Efforts were, therefore, then taken to circumvent the difficulties by implanting and activating dopant ions before the oxide growth. For preserving the GaAs surface and preventing evaporation of As from the surface during the high temperature activation annealing, several approaches were employed.[5,6] One was to grow AlGaAs, SiO_2, and other insulators as cap layers on GaAs, with the etching of those cap layers after the activation. Another way was to activate the implantation with the implanted GaAs wafers annealed at the high temperature under AsH_3 flux in a gas source molecular beam epitaxy chamber. Using both approaches, the annealed GaAs surface was still rough, it lost the atomic ordering, and was not recovered with annealing to ~600 °C under an arsenic overpressure in a MBE chamber, as evidenced from the observation of almost no reflection high-energy electron diffraction (RHEED) patterns, or very faint spotty ones. Note that a good GaAs surface should have streaky 2×4 reconstructed RHEED patterns with annealing under an arsenic environment. The rough GaAs surface perhaps was caused by the diffusion/interaction between the cap layers and GaAs, and loss of arsenic from the surface during the high temperature annealing. Another drawback of ion implanting and activating prior to the oxide growth is that the devices cannot be reduced to a small scale because no self-aligned process was allowed with the approach.

More recently, inversion-channel GaAs MOSFETs using $Ga_2O_3(Gd_2O_3)$ as a gate dielectric were fabricated with the oxide growth, implantation, and activation annealing (~780 °C) in a successive sequence.[7] Even with the expected interfacial roughness between the oxide and GaAs, the latter devices showed better performance than the early devices in terms of drain currents and transconductance. However, the performance of these devices with a gate length of ~1 μm, needs to be improved further to ranges of 20 mA and 100 mS/mm in drain currents and transconductance, respectively, for commercial applications.

For the device processing, $Ga_2O_3(Gd_2O_3)$ should be thermodynamically stable with GaAs at temperatures of ~750 °C or above. The interfacial roughness has to be controlled and minimized to a few angstrom, as was witnessed in the case of the perfected SiO_2–Si interface. However, it was found out later that when the samples are exposed to air, they absorb water and form hydro-oxides.[8] During the annealing process, the hydro-oxides or other contaminations in

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TABLE I. X-ray reflectivity studies on $Ga_2O_3(Gd_2O_3)$/GaAs.

Sample No.	Oxide thickness (nm)	Thermal process	Air-oxide surface roughness (nm)	Interfacial roughness (nm)
A	26.1	Annealed to 780 °C in UHV directly	0.648	0.17
B	25	Exposed to air, then put back to UHV system, remained at 300 °C for 30 min before annealing to 780 °C	0.466	0.14

the oxides, not the pure $Ga_2O_3(Gd_2O_3)$, react with GaAs, resulting in rough interfaces.

In this work, the thermodynamic stability of $Ga_2O_3(Gd_2O_3)$, not the hydro-oxides, with GaAs upon the ultrahigh vacuum (UHV) annealing has been studied using structural and morphological probing tools of x-ray reflectivity (XRR), atomic force microscopy (AFM), and cross-sectional high-resolution transmission electron microscopy (HRTEM). The results have revealed that the interface between $Ga_2O_3(Gd_2O_3)$ and GaAs remains intact with the annealing temperatures up to 780 °C and the interfacial roughness is less than 0.2 nm, a value close to that of the SiO_2-Si interface. Moreover, $Ga_2O_3(Gd_2O_3)$ remains amorphous with the high temperature annealing, an important aspect for high κ gate dielectrics. Current-voltage ($I-V$) and capacitance-voltage ($C-V$) measurements showed that the leakage currents through the oxide and the D_{it}'s remain low with the samples annealed at high temperatures.

All the samples were prepared in a multichamber system, which includes a solid source GaAs-based MBE chamber, an oxide deposition chamber and UHV transfer modules. First, GaAs epitaxial layers doped with Si in 4×10^{17} cm^{-3} were prepared in the solid-source MBE chamber. The wafers were then transferred *in situ* under a vacuum of 10^{-10} Torr to the oxide chamber for $Ga_2O_3(Gd_2O_3)$ deposition. A detailed procedure in the oxide growth was given earlier.[3]

Two oxide samples were annealed in different ways for comparison. After the oxide growth, the first sample (sample A) was directly heated to 780 °C in the UHV system without exposing to air. The other sample was moved out of the UHV system and exposed to the high humidity environment of Taiwan for more than 100 days. Then, the sample (sample B) was moved back to the UHV system for the thermal processes: Being ramped up to 300 °C and remaining there for 30 min to get rid of the water contained in the film, and then heated up to 780 °C in 5 min. The details of different thermal process on each sample are listed in Table I. Note that a severe thermal budget was put on the samples, compared with the usual rapid thermal annealing. After the high temperature (780 °C) annealing process, the RHEED pattern indicates that the sample remains to be amorphous.

The MOS diode structure was fabricated by evaporating Au dots 0.1 mm in diameter. $I-V$ and $C-V$ characteristics were measured using Agilent 4156C and 4284, respectively. Electrical measurement and transmission electron microscopy were also used to investigate the oxide integrity after the high temperature annealing.

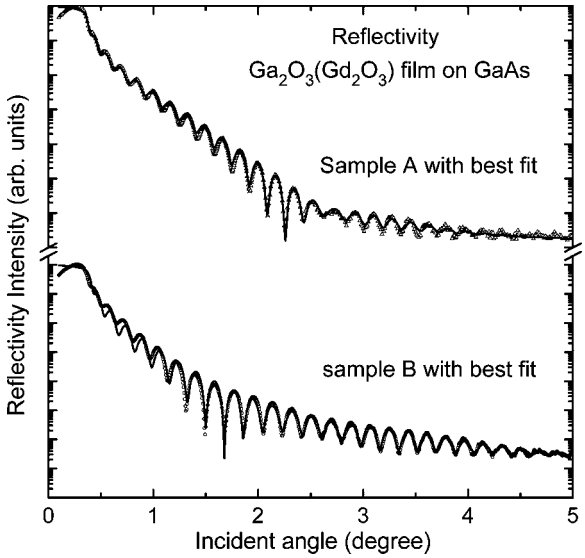

FIG. 1. Low angle x-ray reflectivity of Ga_2O_3 (Gd_2O_3) on GaAs annealing in UHV, with experimental data (dots) and a theoretical fit (line).

XRR measurements were performed using Cu $K\alpha$ radiation in a standard Huber four-circle x-ray diffractometer operated at 50 kV and 200 mA. The incident light was monochromatized by a flat Ge(111) crystal and two sets of slits were used to eliminate Cu $K\alpha_2$ contamination and obtained a wave-vector resolution in the scattering plane of the order 0.015 nm^{-1}. The detailed experimental setup for XRR measurement was described elsewhere.[9] The theory of specular reflectivity is based on the recursive formalism of Parratt.[10] To determine physical parameters of the film such as interfacial roughness, thickness and electron density,[11] the reflectivity data were fitted with the $Bede_{REFS}$ MERCURY code.[12]

As illustrated in Fig. 1, the x-ray reflectivity observed on the two samples annealed in UHV but in different conditions showed a well-behaved fringe pattern. From the period of oscillations, the oxide film thickness has been accurately calculated. The values of the roughness of the oxide surface and the interface between the oxide and GaAs have also been calculated using the theoretical fitting model. Table I lists the fitting results for the samples with the two different thermal processes. A very small interfacial roughness of <0.2 nm has been obtained in the interface of $Ga_2O_3(Gd_2O_3)-GaAs$ after UHV annealing.

Remaining at 300 °C for 30 min in UHV allowed the hydro-oxides to be removed from the air-exposed sample B, as evidenced from a rapid increase of the amount of H_2O contained in the chamber, detected using a residual gas ana-

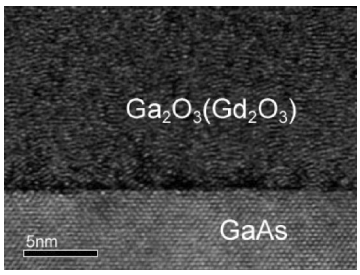

FIG. 2. High-resolution cross-sectional TEM picture of $Ga_2O_3(Gd_2O_3)$ on GaAs after air exposure and annealing in UHV (sample B).

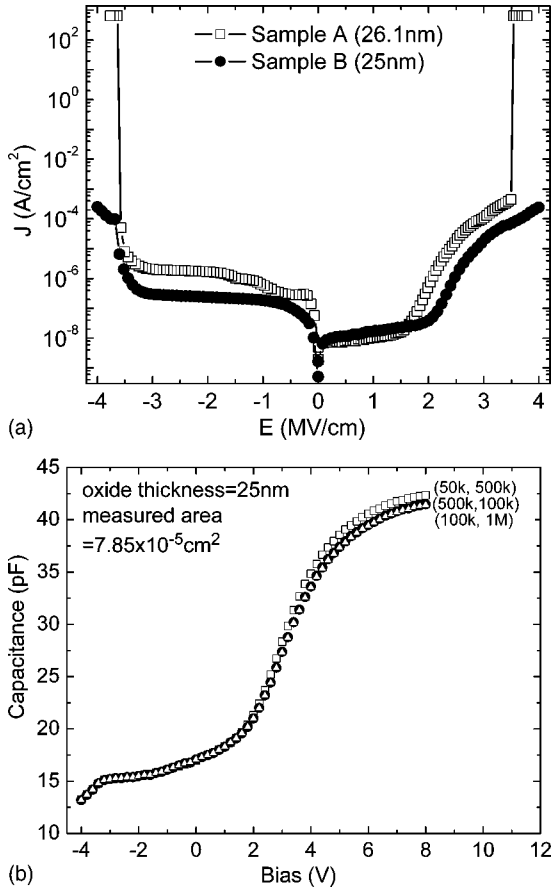

FIG. 3. (a) Leakage current density J (A/cm^2) vs E (MV/cm) for $Ga_2O_3(Gd_2O_3)$/GaAs samples in different thermal processes and (b) $C-V$ curves of a MOS diode made of $Au/Ga_2O_3(Gd_2O_3)$ (25 nm)/GaAs after two-frequency corrections (sample B).

lyzer. The consequent annealing to high temperatures let GaAs be adjacent to hydro-oxide free $Ga_2O_3(Gd_2O_3)$.

Figure 2 shows a high-resolution cross-sectional TEM picture of the sample B, in which $Ga_2O_3(Gd_2O_3)$ remains amorphous. The oxide thickness measured by the TEM is 25.2 nm, in agreement with the XRR data. A sharp transition from GaAs to $Ga_2O_3(Gd_2O_3)$ was observed. Even after being exposed to air for more than 100 days and absorbing water vapor, the hydro-oxides in the film were driven out with the 300 °C annealing in UHV. The root mean square roughness of the surface (measured by AFM) averaged over 3 μm $\times 3$ μm area is smaller than 0.35 nm, which is slightly less than the values obtained from the reflectivity measurements.

Figure 3(a) of the current density–electrical field ($J-E$) curves for the two samples shows a leakage current density of $Ga_2O_3(Gd_2O_3)$ on GaAs of about $10^{-8}-10^{-9}$ A/cm^2 at low gate voltages. J is the current density with I divided by the area of the Au dot and E is the electrical field with V divided by the oxide thickness. The electrical breakdown fields are almost 4 MV/cm and are symmetrical on both positive and negative biasing. $C-V$ curves were obtained with frequencies varying from 1 kHz to 1 MHz and the dispersion in the $C-V$ curves of different frequencies was due to the equivalent circuit of complex impedance. An improved two-frequency method was used to correct the results[13] as shown in Fig. 3(b). Capacitances were calculated by the four-element model for different pairs of frequencies. The dielectric constant of $Ga_2O_3(Gd_2O_3)$ is calculated to be about 15.11. The D_{it} was estimated to be less than $\sim 10^{12}$ cm^{-2} eV^{-1} using the Terman method.[14]

In conclusion, the studies using XRR and HRTEM have shown that an atomically abrupt and smooth $Ga_2O_3(Gd_2O_3)$/GaAs interface has been achieved after high temperature (780 °C) annealing in UHV and the oxide remains amorphous. This has demonstrated that $Ga_2O_3(Gd_2O_3)$ dielectric films deposited on GaAs are indeed thermodynamically stable at high temperatures. Further, $J-E$ and $C-V$ measurements also show the excellent electrical properties of the annealed $Ga_2O_3(Gd_2O_3)$/GaAs, having low D_{it}, low leakage currents, and high dielectric constant.

The rough surfaces and $Ga_2O_3(Gd_2O_3)$/GaAs interfaces encountered previously during the high temperature annealing were caused mainly by the hydro-oxide formation, which occurs during air exposure of the dielectric films. The hydro-oxide formation has caused the oxide deterioration and more harmfully the interaction between the film and the substrate. The attainment of a smooth interface between the gate dielectric and GaAs after high-temperature annealing is essential to ensure the low D_{it} and maintain a high carrier mobility in the channel of the MOSFET. Our findings enable fabrication of high-performance inversion channel GaAs-based MOSFETs.

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